BlueICe

Your ideas into Silicon

BluSignalProcessor,
BLUSP
A novel Ultra low power processor core.

Leon Cloetens, BlueICe

Amsterdam, june 12 2013

Agenda

- Few words about BluelCe
- Market opportunity in medium data rate communication technologies
- Overall BluelCe platform
- BluSP signal processing architecture
  - Features
  - Performance
- Conclusion – further steps

BlueICe

- founded 2010
- SOC and IP micro-electronics design services company
  - Mastering (also through partnerships) all the competences to build a complete SOC
  - Differentiating through focus on system and architecture, with a special focus on communication solutions, wireless in particular
    - Ultra low power is key
  - Differentiating through processor based, programmable architectures
    - Ultra low power is key

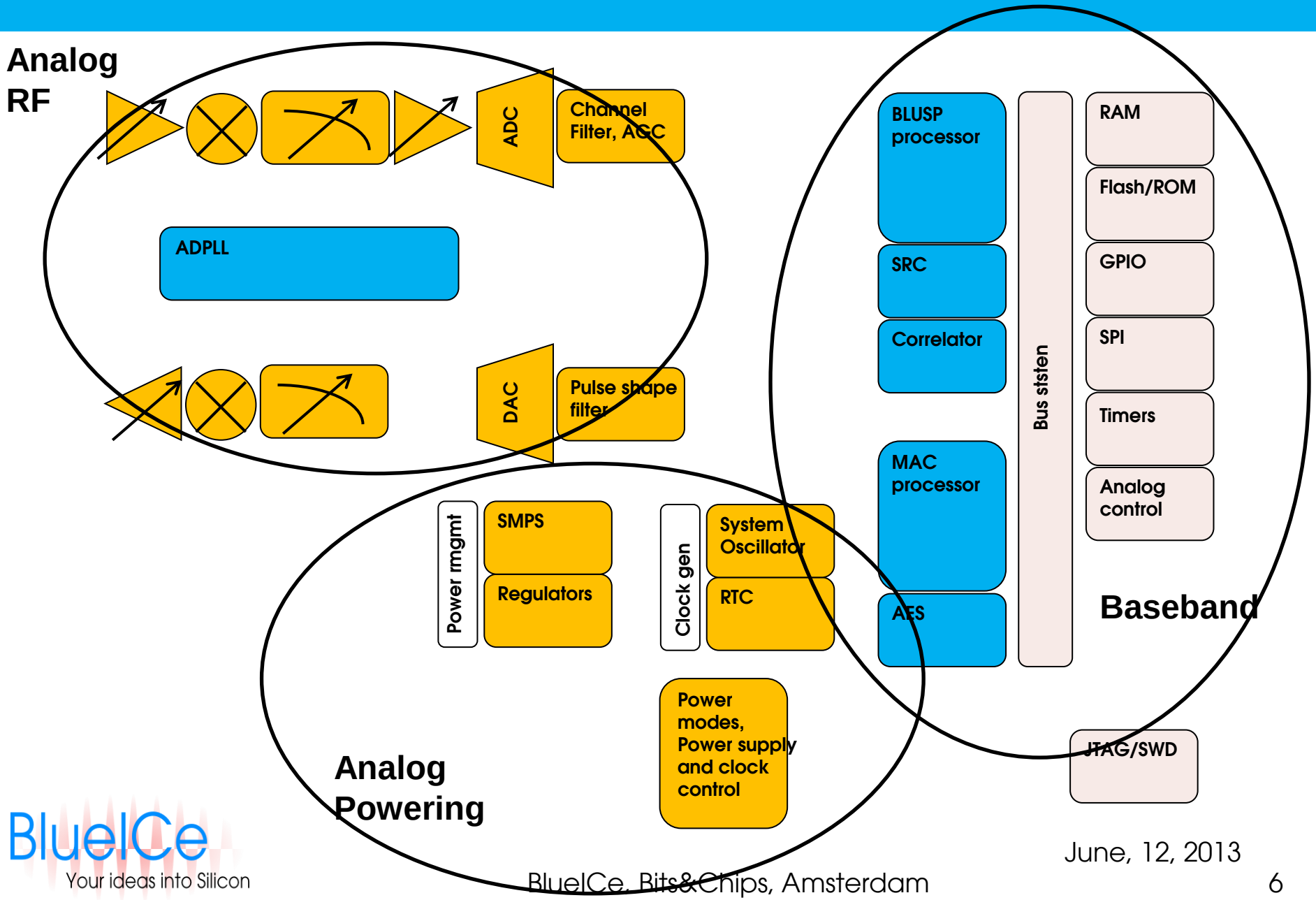
BlueICe

- ~10 people size
- Located around Brussels with a small subsidiary in Shuzou-China
- Invested in a number of IP's among which our own processor architecture: BluSP
- Invested in a tool-chain for this core, in cooperation with BlueBee, a spin-off from TU-Delft
- Partnership in place with IMEC Services giving us library and silicon access to TSMC technology
- Working together with several customers in wireless and ultra low power type of applications

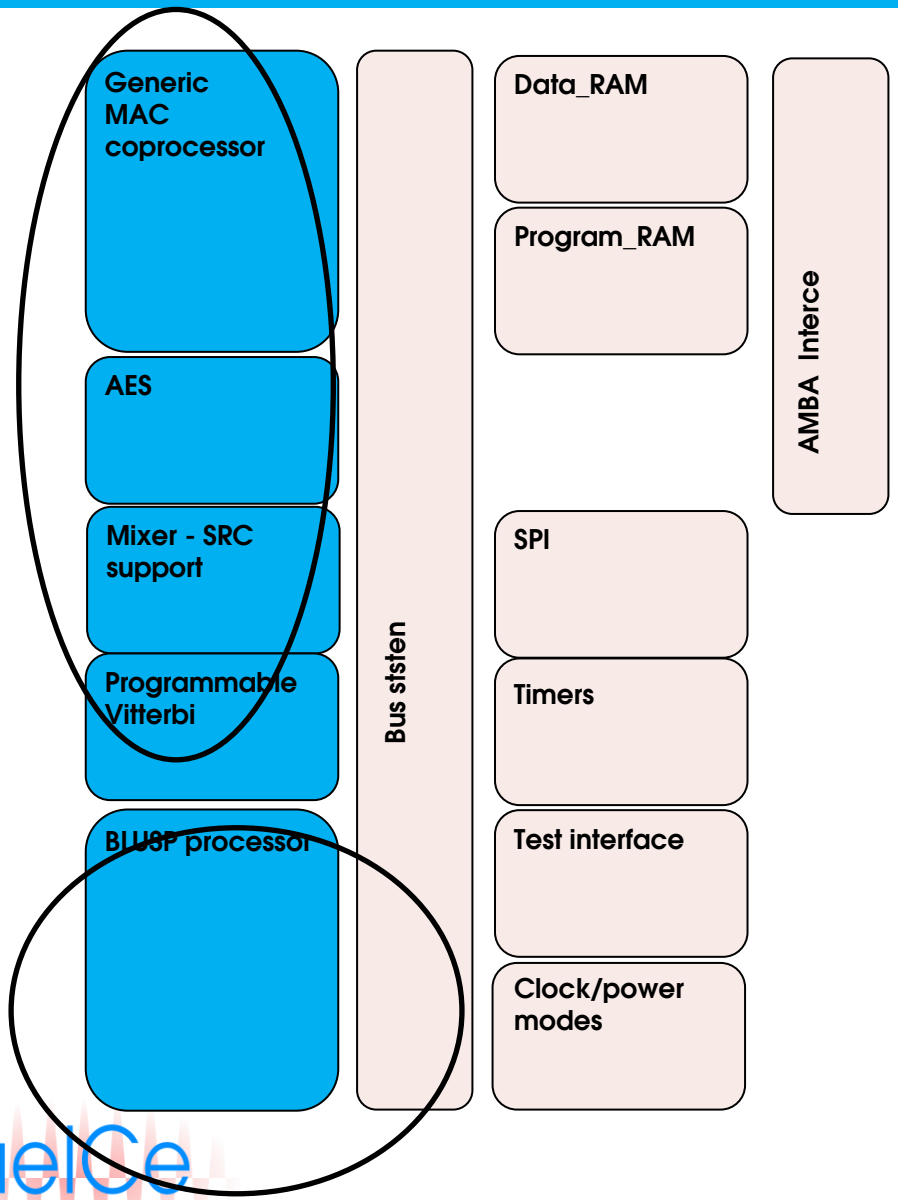
BlueICe vision of medium data rate wireless architecture (1)

- Medium data-rate means for us: 1 to 20Mbit/s
- Application examples
  - Future 802.15.4 wireless industrial technology
  - Future 802.11.ah – WIFI - subGhz wireless technology
  - Ultra low power standard WIFI, 802.11.n
  - Power Line Carrier
- Ultra low power is key (new) requirement
  - Battery fed with target battery lifetimes of 5years+ (new)
- Flexible if possible – now most solutions are hardwired
  - Eases development
  - Copes with evolving standards…

Wireless [OFDM], Overall Tranceiver Architecture



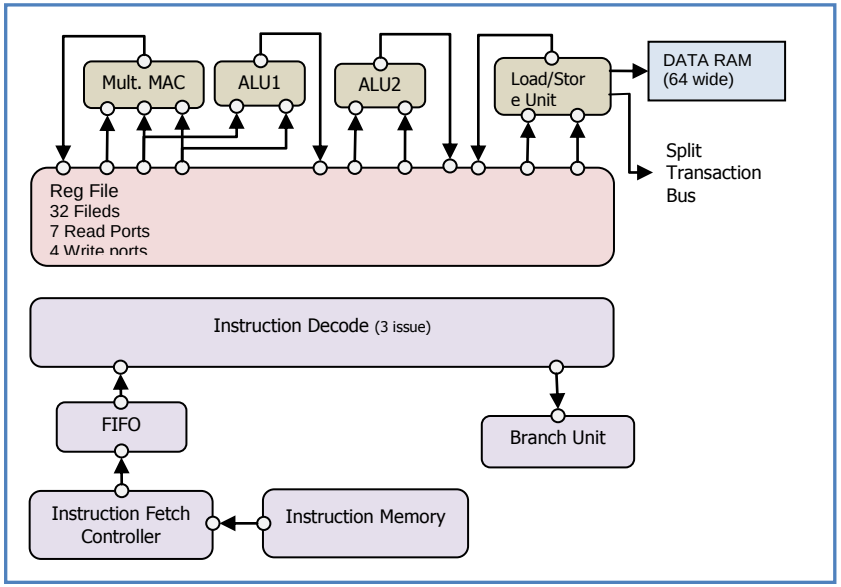
Baseband architecture



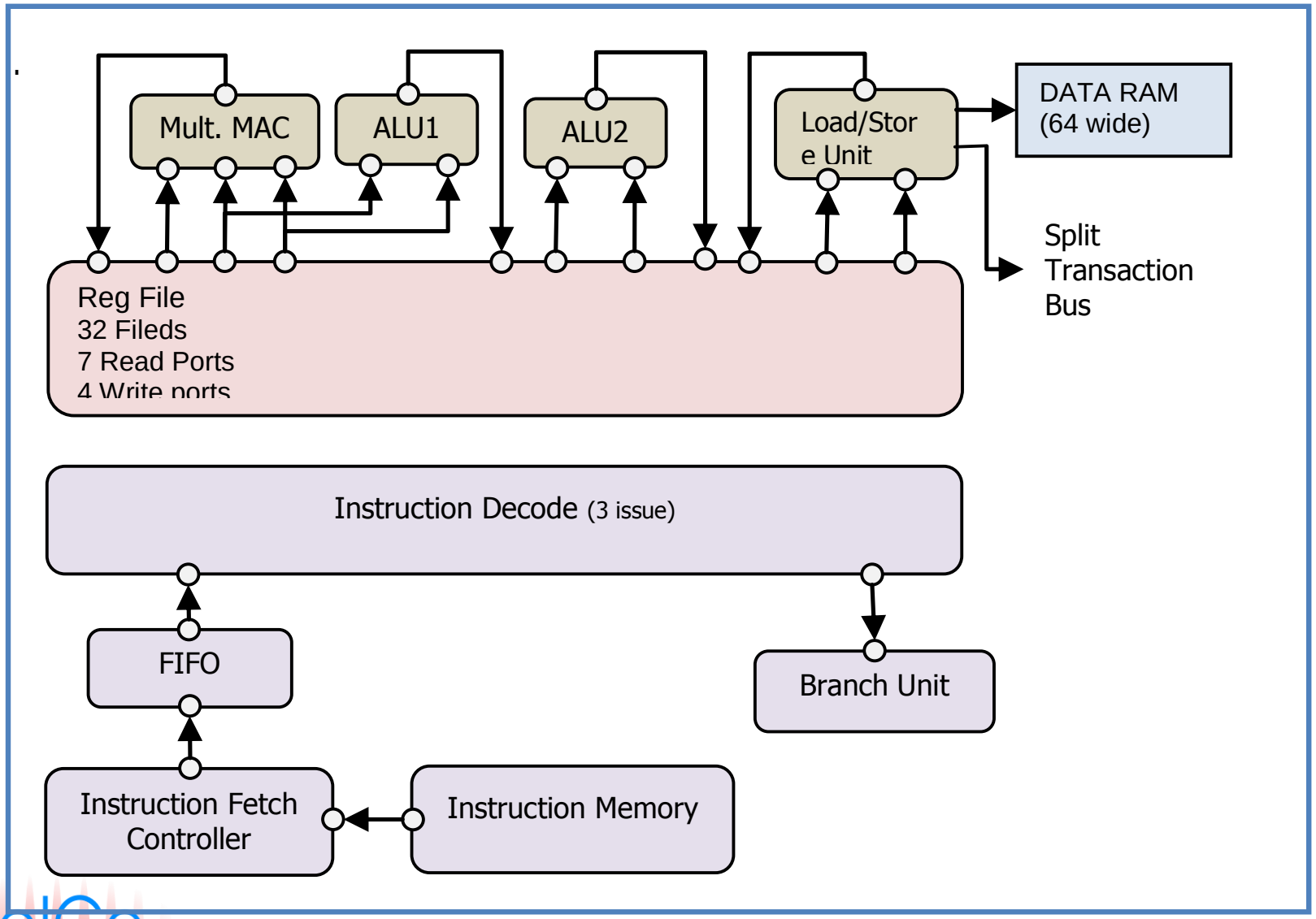
- Coprocessors are required for performance
- BLUSP brings flexibility
- Network on Chip
  - Significant in multiprocessor architecture
- "Standard infrastructure"
  - reuse

BluSP architecture Architectural choices make it fast and very low power

- 3 Issue 32 bits core
- True Risk - Relatively limited instruction set: <100
- Single cycle complex MAC at 16Bits
- Large 32 bit register file, reducing amount of memory accesses
- Very advanced clock gating



BluSP architecture



Power consumption data

- 70kgates
- **> 600 Mhz** speed in a 40nm LP library
- Power consumption in a **40nm LP** TSMC library, operated at 1.1Volts:
  - **13uA/Mhz** with a typical program.
  - 21uA/Mhz with a "smoker" pattern.
    - This pattern is loading the slots and the complex MAC at 100%
  - These data are based on simulations with **post layout** extraction of load capacitances and resistances

Tool strategy

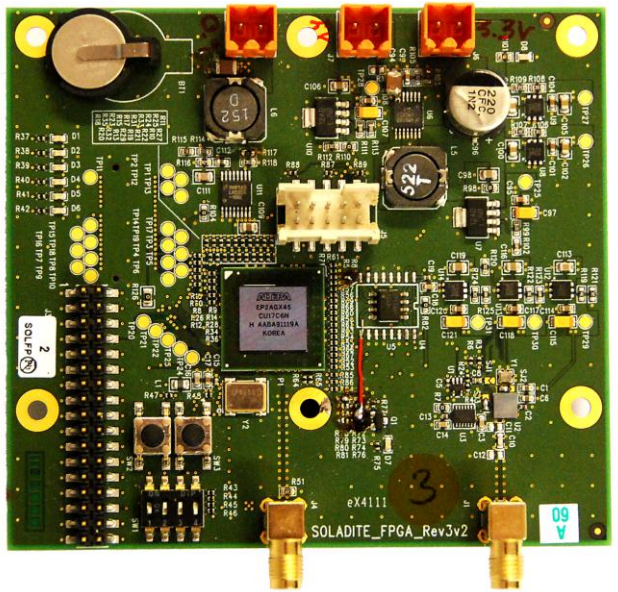
- **ECLIPS based** software development kit
  - Comprised of a (assembly) code simulator, debugger, profiler, compiler.
- Developed in cooperation with an external partner
  - GNU based
  - BlueBee, as spin-off from TU-Delft
- Small, ultra RISC, instruction set with few (only one) specific data type -> makes it **very easy** to optimize **standard C code** for the core
- Achieved 90% code density on compiling a Cortex Mx based Bluetooth stack, vs. top notch ARM standard compilers

Code efficiency benchmarks

- Its calculation power and speed make it fit to implement also complex and high data rate modulation applications
  - It can e.g. handle a **256 point FFT** in **1350 cycles** with 16bit precision
- Its 32 bit capability make it fit to handle audio applications
  - The core can implement in 32bit an **MP3** decoder, running at **4Mhz clock rate**

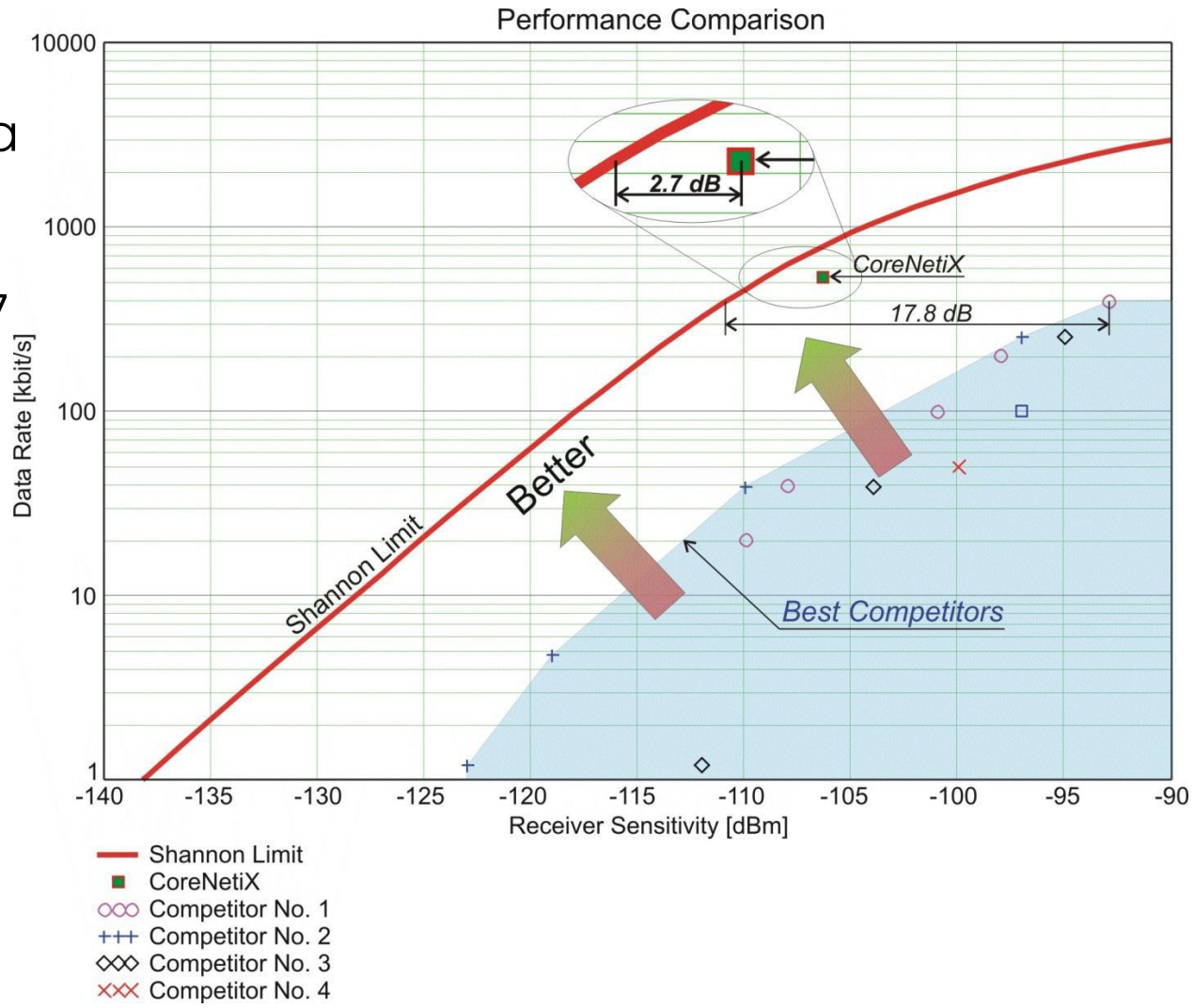
Target application domains

- Communication
  - PHY processing
  - Especially for OFDM and alike technology which require an efficient mix of complex and time domain calculation
  - It's efficient "glue code" performance make it also fit for MAC processing
- Image processing
  - Image/object recognition
  - Characterized by a mix of DSP and glue – heuristic code
- RADAR receivers



Application example

- Demonstrated the core with a (CoreNetiX) High Data Rate solution offers extraordinary performance: only 2.7 dB worse than theoretical limit.
- Leveraging the processor and the coprocessor of the complete solution



Conclusion – further work

- BluSP is an excellent compromise between calculation power and low power performance
  - Customer benchmarks confirming this
- Future work
  - Looking for application partners especially in the non communication domain
  - Imaging
  - RADAR
- Participating in a research program to let it evolve into a multiprocessor architecture